Error (10170): Verilog HDL syntax error at texter\_control.v(36) near text: "=". Check for and fix any syntax errors that appear immediately before or at the specified keyword. The Intel FPGA Knowledge Database contains many articles with specific details on how to resolve this error. Visit the Knowledge Database at https://www.altera.com/support/support-resources/knowledge-base/search.html and search for this specific error message number.

Error (10170): Verilog HDL syntax error at texter\_control.v(43) near text: "if"; expecting "endcase". Check for and fix any syntax errors that appear immediately before or at the specified keyword. The Intel FPGA Knowledge Database contains many articles with specific details on how to resolve this error. Visit the Knowledge Database at https://www.altera.com/support/support-resources/knowledge-base/search.html and search for this specific error message number.

// Single Button Texter -- texter control module

// -- texter\_control.v file

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//

// This is the main texter\_control module for the single button texter.

// This module should implement the design that was described by the

// ASM Chart that was presented in Laboratory 10 of the CPE 324 class.

// The design is to be reset to state S0 whenever the reset signal is

// at a logic high. Whenever the reset signal is at a logic low it

// should fully implement the state machine specified by the SM chart.

// The clock signal is assumed to be a 50% duty cycle clock that is the

// same clock that drives the other functional units that

// are being controlled by this module (50 Mhz on the DE2-115). The other

// input and output signals are all assumed to be active high. The

// input signal, sw, is controlled by the user and the other inputs

// are status inputs that come directly from the functional units

// that are being controlled. These inputs will change their states in

// direct response to your controlling outputs that you provide. The

// outputs are all assumed to be active for a one clock duration as

// indicated by the ASM chart.

module texter\_control(input clk, reset, sw, space, dash\_dit, dc\_error,

output reg nxt\_bit, nxt\_char, out\_char, out\_space, tm\_reset,

sp\_load, back\_sp);

reg [2:0] state=0, next\_state=0;

// S0 to S5 states (6 cases)

always @ (state, reset, sw, space, dash\_dit, dc\_error)

begin

nxt\_bit=0; nxt\_char=0; out\_char=0; out\_space=0; tm\_reset=0; sp\_load=0; back\_sp=0;

if (reset) next\_state=0;

else

case(state)

0: if (sw) begin tm\_reset=1; nxt\_char=1; next\_state=1; end

else begin next\_state=0; end

1: if (sw) next\_state=1;

else

if (space) begin back\_sp=1; next\_state=0; end

else

begin

nxt\_bit=1;

if (dash\_dit) begin sp\_load=1; next\_state=2; end

else next\_state=2;

end

2: begin tm\_reset=1; next\_state=3; end

3: if (sw) begin sp\_load=1; next\_state=4; end

else

if (!dash\_dit) next\_state=3;

else

if (dc\_error) next\_state=0;

else begin out\_char=1; next\_state=5; end

4: begin tm\_reset=1; next\_state=1; end

5: if (sw) begin nxt\_char=1; tm\_reset=1; next\_state=1; end

else

if (space) begin out\_space=1; next\_state=0; end

else next\_state=5;

endcase

end

always @ (posedge clk)

state = next\_state;

endmodule

Warning (18236): Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM\_PARALLEL\_PROCESSORS in your QSF to an appropriate value for best performance.

Warning (10230): Verilog HDL assignment warning at sw\_driver.v(146): truncated value with size 32 to match size of target (23)

Warning (10030): Net "m\_clk\_range.data\_a" at sw\_driver.v(13) has no driver or initial value, using a default initial value '0'

Warning (127007): Memory Initialization File or Hexadecimal (Intel-Format) File "C:/Users/eas0035/Documents/lab5/db/lab5\_ptb.ram0\_usend\_78d4ead.hdl.mif" contains "don't care" values -- overwriting them with 0s

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